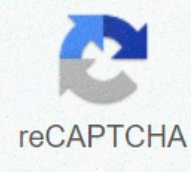




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Operational amplifier notes pdf

High Gain Voltage Amplifier with Differential Input Op Amp A μ A741 Integrated Circuit One Type of Most Successful Op Amp First Production 1967 Pin Configuration V+ : Non-Inverted Input V- : Inverted Input V-out: Output VS+ : Plus Power VS- : Negative Power Supply Power Terminal (VS+ and VS-) Power Pins (see IC Power Pins) can be labeled separately. In many cases, these pins are left out of the diagram for clarity, and the power configuration is described or assumed from the circuit. For electronic symbol schematic symbols on amplifiers, the pin is labeled above. Op amps (op amps and op amps) are DC-coupled high-interest electronic voltage amplifiers with differential inputs and usually single-ended outputs. [1] In this configuration, the op amp generates an output potential (for circuit grounding) and is usually 100,000 times the potential difference between the input terminals. Op amps originated in analog computers and were used to perform mathematical operations on linear, nonlinear, and frequency-dependent circuits. The popularity of op amps as building blocks of analog circuits is due to their versatility. By using negative feedback, the characteristics of the op amp circuit, its gain, input and output impedance, bandwidth, etc. are determined by the external components and are almost independent of the temperature coefficients and engineering tolerances of the op amp itself. Op amplifiers are widely used in electronic devices today, including a vast array of consumer, industrial and scientific instruments. Many standard IC op amps cost only a few cents. However, some integrated or hybrid op amps with special performance specifications may cost more than USD 100 in small quantities. [2] Op amps can be packaged as a component or used as an element of a more complex integrated circuit. Op amps are one type of differential amplifier. Other types of differential amplifiers include full differential amplifiers (similar to op amps, but with two outputs), instrumentation amplifiers (usually built from three op amps), insulated amplifiers (usually tolerances for common mode voltages that destroy normal op amps), and negative feedback amplifiers (usually built from one or more op amps and resistance networks). Operation The differential input of an op amp (comparator) amplifier without negative feedback consists of a non-inverting input (+) with a voltage V+ and an inverted input (-) with a voltage V-. Ideally, the op amp amplifies only the difference in voltage between the two, called the differential input voltage. The output voltage of the op amp Vout is given by the formula Vout, which is the open loop gain of the expression Vout. A $O_L(V^+ - V^-)$ in the display style $V_o = V_o = V_o$.

(The term open loop refers to the lack of an external feedback loop from output to input.) The size of the open-loop amplifier AOL is generally very large (more than 100,000 for integrated circuit op amp) so even when V+ and V-, the amplifier output is close to the supply voltage. A situation in which the output voltage is greater than or greater than the supply voltage is called the saturation of the amplifier. Since the size of the AOL is not sufficiently controlled in the manufacturing process, it is not practical to use an open loop amplifier as a stand-alone differential amplifier. Without negative feedback, and perhaps with positive feedback for playback, the op amp will function as a comparator. If the inverted input is held directly on the ground (0 V) or by the resistor Rg, and the input voltage Vin applied to the non-inverted input is positive, the output is maximum positive. If Vin is negative, the output is maximum negative. Since there is no feedback on either input from the output, it is an open loop circuit that functions as a comparator. If the operation amplifier having a closed-loop amplification (non-inverting amplifier) (non-inverting amplifier) predictable operation is desirable, negative feedback is used, applying a portion of the output voltage to the inverted input. Closed-loop feedback significantly reduces the gain of the circuit. With negative feedback, the gain and response of the entire circuit is determined by the feedback network, not by the op amp characteristics. If the feedback network consists of components with a lower value for the input impedance of the op amp, the value of the open loop response AOL of the op amp does not seriously affect the performance of the circuit. The response of the op amp circuit to the input input, the output, and the feedback circuit is mathematically characterized by the transfer function. Designing an op amp circuit with the desired transmission function is in the field of electrical engineering. The transfer function is important for most applications of op amps, such as analog computers. High input impedance at the input terminal and low output impedance at the output terminal are particularly useful functions of the op amp. In the right non-inverting amplifier, the presence of negative feedback via the voltage divider Rf, Rg determines the closed-loop gain ACL Vout/Vin. If Vout is sufficient to reach and pull the inverted input to the same voltage as Vin, equilibrium is established. The voltage gain of the entire circuit is therefore 1 + Rf/Rg. As a simple example, if Vin is 1 V and Rf is Rg, Vout is 2 V, which is the same amount that is required to keep V- at 1 V. For feedback provided by the Rf, Rg network, this is a closed-loop circuit. Another method of analyzing this circuit proceeds by performing the following (usually valid) assumptions: [3] If the op amp operates in linear (i.e., not saturated) mode, the difference is as follows: The difference between the inverted pin (+) and the inverted (-) pin is very small. The input impedance between the (+) and (-) pins is much greater than the other resistors in the circuit. The input signal Vin appears on both the (+) and (-) pins, resulting in currents i through Rg equal to Vin/Rg: I in the current method of Kirtchoff, the same current must leave the node when the node is entered, and (-) because the impedance to the pin is close to infinity. It can be assumed that the current i flows through Rf, the output voltage Vout, $V_{in} + i R_f$, $V_{in} + R_f R_{in} V_{in} / R_{in} V_{in}$.

V. The ideal op amp is usually considered to have the following characteristics: [4][5] Infinite Open Loop Gain G -vout/vin Infinite Input Impedance Phosphorus, Zero Input Zero Output Voltage Range Bandwidth Zero Phase Shift and Infinite Slew Rate Zero Output Impedance Zero Noise Immunity Common Mode Rejection Ratio (CMRR) Infinite Power Rejection Ratio. These ideals can be summarized by two golden rules: in a closed loop the output will try to do whatever is necessary to zero the voltage difference between the inputs. The input does not draw current. [6][17] The first rule applies only if op amp is normally used in a closed-loop design (negative feedback, returns some signal path from the output to the inverted input). These rules are commonly used as the first approximation suitable for the analysis and design of op amp circuits. [6]:177 Note that these ideals can be fully realized. The actual op amp can be modeled with non-infinite or non-zero parameters using the equivalent resistance and capacitor of the op amp model. Designers can include these effects in the overall performance of the final circuit. Some parameters have a negligible effect on the final design, while others represent the actual limits of final performance that need to be evaluated. Real Op Real Op Amps are different from ideal models in many ways. DC Imperfection The actual op amp suffers from some non-ideal effects: the finite gain open loop gain is infinite in the ideal op amp, but finite in the actual op amp. A typical device shows an open loop DC gain in the range of 100,000 to more than 1 million. AsThe loop gain (i.e., the product of open loop and feedback gain) is very large, and the circuit gain is completely determined by the amount of negative feedback (i.e., independent of the open loop gain). If the closed loop gain must be very high, the feedback gain is very low and the low feedback gain causes a low loop gain. In these cases, the op amp will not work ideally. Finite input impedance The differential input impedance of an op amp is defined as the impedance between the two inputs. The common mode input impedance is the impedance from each input to the ground. Because MOSFET input amplifiers have a protection circuit that effectively short-circuits input differences larger than small thresholds, some tests may appear to have very low input impedance. However, as long as these op amps are used in a typical high gain application, these protection circuits will be dead weights. The input bias and leakage currents described below are more important design parameters for typical op amp applications. Non-zero output impedance Low output impedance is important for low impedance loads. For these loads, the voltage drop across the output impedance effectively reduces the open loop gain. In a configuration with voltage sensing negative feedback, the output impedance of the amplifier is effectively reduced. Therefore, in linear applications, the op amp circuit typically shows a very low output impedance. Low impedance output typically require high static (idle) current at the output stage and dissipates more power, which can intentionally sacrifice low output impedance in low-power designs. The input current matches and the impedance looking out of both inputs matches, the voltage generated by each input is equal. These matching voltages have no effect because the op amp operates against the difference between inputs. It is more common for the input current to be a little mismatched. The difference is called the input offset current, and even a matched resistor can produce a small offset voltage (different from the input offset voltage below). This offset voltage allows you to create offsets and drifts in the op amp. Input offset voltage This is the voltage required across the input terminal of the op amp to drive the output voltage to zero. [7] [nb 1] In a perfect amplifier, there is no input offset voltage. But it's present in the actual op ampAmplifiers that make up the input phase for the majority of these devices. The input offset voltage causes two problems: first, the amplifier's high voltage gain effectively ensures that the amplifier output is saturated if it operates without negative feedback, even when the input terminals are wired. Second, in the closed loop, the negative feedback configuration, the input offset voltage is amplified with the signal, if high-precision DC amplification is required, or may cause problems when the input signal is very small. [nb 2] Common mode gain Perfect op amp amplifies only the voltage difference between the two inputs and completely rejects all voltages common to both. However, since the differential input stage of the op amp is not perfect, these common voltages are amplified to some extent. The standard measure of this defect is called the common mode rejection rate (called CMRR). Minimizing common-mode gain is usually important for non-inverting amplifiers that operate at high amplification (see below). The output of the power denied perfect op amp is completely independent of its power supply. All actual op amps have a finite power removal ratio (PSRR) that reflects how well the op amp can reject changes in the supply voltage. Temperature effect All parameters vary depending on the temperature. The temperature drift of the input offset voltage is particularly important. Drift real op amp parameters may receive slow changes in temperature, input conditions, etc. over time. The gain of the op amp calculated by the defective DC of the AC does not apply at higher frequencies. Therefore, for fast operation, more advanced considerations should be used in the op-amp circuit design. Finite bandwidth All amplifiers have finite bandwidth. To the first approximation, the op amp has a frequency response of the integrator with gain. In other words, the gain of a typical op amp is inversely proportional to the frequency and is characterized by its gain bandwidth product (GBWP). For example, an op amp with a 1 MHz GBWP has a gain of 5 at 200 kHz and a gain of 1 at 1 MHz. Combined with the very high DC gain of the op amp, this dynamic response is the characteristics of the first low-pass filter with very high DC gain and low cutoff frequency divided by DC gain. The same bandwidth of the op amp may cause several problems, such as: associated with the limit of the stability bandwidth is a phase difference between the input signal and the amplifier output, which may lead to oscillation in some feedback circuits.

For example, when 180 degrees late to form a positive feedback, sine wave output signal which means that interferes destructively with the input signal of the same frequency is constructively interfered. In such cases, the feedback circuit can be stabilized in the following ways:Correction increases the gain or phase margin of the open loop circuit. Circuit designers can implement this correction externally using a different circuit component, alternatively, compensation can be made within the op amp by adding a dominant pole that sufficiently attenuates the high-frequency gain of the op amp. The position of the pole can be configured by the circuit designer using either internally fixed by the manufacturer or implemented using a method specific to the op amp. In general, dominant pole frequency compensation further reduces the bandwidth of the op amp. If the desired closed-loop gain is high, op frequency compensation is often not required because the required open loop gain is low enough. Therefore, applications with high closed-loop gain can take advantage of op amps with higher bandwidth. Distortion and other effectsSevered bandwidth outputs impedance as the skewness increases and the frequency increases because of the low amount of feedback at high frequencies. A typical low-cost, general-purpose op amp shows GBWP of several megahertz. There are special and high-speed op amps that can achieve GBWP of hundreds of megahertz. Current feedback amplifiers are often used in very high frequency circuits. The noise amplifier generates a random voltage at output, even if no signal is applied. This may be due to the thermal noise and flickering noise of the device. Noise is a very important consideration for high-gain or high-bandwidth amplifiers. It is most important for high-frequency operation because it reduces the input capacity input impedance and can cause phase shift. Common mode gain See DC imperfections above. As the power-denied frequency increases, the power rejection usually worsens. Therefore, it is important to keep the signal supply clean with higher frequency ripples, such as the use of bypass capacitors. Nonlinear Defects Inverted Amplifier Saturation Amplifier Saturated Op amp inputs (yellow) and output (green) are limited to a minimum and maximum value close to the supply voltage. [nb 3] The output of the old op amp can reach within one or two bolts of the power rail. The output of the new so-called rail-to-rail op amp can reach within the millivolt of the power rail when supplying low output current. The output voltage of the through amplifier usually reaches the slew rate, which is the maximum rate of change specified in the number of volts per microsecond (V/μs). Further increases in the input signal will no longer affect the rate of change in the output, though is usually caused by the saturation of the output stage. As a result, there is a constant current driving the capacitance C (especially the capacitance used to implement frequency compensation) in the amplifier. The slew rate is limited by the IC, slew rate and is associated with the large signal performance of the op amp.For example, an op amp with a gain of 10. Make the input a 1 V, 100 kHz serrated wave. In other words, the amplitude is 1 V and the duration is 10 microseconds. Therefore, the rate of change in the input (i.e., slope) is 0.1 V per microsecond. After × 10-inch amplification, the output must be 10 V, 100 kHz serrated and must have a corresponding slew rate of 1 V per microsecond. However, the classic 741 op amp has a microsecond slew rate specification of 0.5 V so that its output can be increased to 5 V or less in a period of 10 microseconds of saws. Therefore, when measuring the output, it will cost 5 V, 100 kHz, rather than a 10 V, 100 kHz saw. Next, consider the same amplifier and 100 kHz saw, but the input amplitude is now 100 mV instead of 1 V. The × output is a 1 V, 100kHz sawtooth with a corresponding slew rate of 0.1 V per microsecond. In this case, 741 with a microsecond slew rate of 0.5V properly amplifies the input. Modern high-speed op amps can have slew rates of more than 5,000 V per microsecond. However, it is common for the slew rate of the op amp to be in the range of 5 to 100 V per microsecond. For example, a general-purpose TL081 op amp has a slew rate of 13V per microsecond. As a rule, low power and low bandwidth op amps have a low slew rate. For example, the LT194A micropower op amp consumes 1.5 micromps, but has a gain bandwidth product of 2.7 kHz and 0.001 V per microsecond slew rate. Nonlinear input output relationship The output voltage may not be exactly proportional to the difference between the input voltages. If the input signal is a waveform, it is commonly referred to as distortion. This effect is very small in practical circuits where substantial negative feedback is used. Phase inversion In some integrated op amps, if the exposed common mode voltage is violated (for example, by one of the inputs driven to one of the supply voltages), the output may turn to the opposite polarity as expected in normal operation. [8] [9] Under such conditions, negative feedback is positive, which may cause the circuit to lock up in that state. Power considerations Limited output current Output current must be finite.

Practice, most op amps are designed to limit the output current to about 25 mA for the type of 741 IC op amp, protecting the op amp and related circuits from damage. The latest design is more electronically robust than a previous implementation, can maintain a direct short circuit without damaging its output. Output sink current The output sink current is the maximum current that the op amp may enter a thermal shutdown or be destroyed. The latest integrated Fet or MOSFET op amp approximates an op amp that is more ideal than bipolar ICs when it comes to input impedance and input bias current. Bipolars are generally superior in regard to input voltage offsets and often have low noise. In general, Fet and MOSFET op amps provide better performance when using fairly large signals at room temperature and bandwidth is limited. The internal circuit of type 741 op amp A is a component level diagram of a typical 741 op amp. Dotted outline: current mirror; An example of a bipolar transistor; op amp, procured by many manufacturers and several similar products, is a 741 integrated circuit designed in 1968 by Fairchild Semiconductor's David Flagler after Bob Widlar's LM301 integrated circuit design. In this discussion, the parameters of the hybrid pin model are used to characterize the small signal and ground emitter characteristics of transistors. In this model, the current gain of the transistor is more commonly called hfe called hie, which is called β, and the 741 op amp, a small integrated circuit, shares with most operations and amplifies the internal structure consisting of three gain stages: [12] Differential amplification (dark blue contour) - common mode signal, low noise, Provides high differential amplification (gain) with rejection of high input input impedance. Drives voltage amplifiers (magenta outline), provides high voltage gain, single-pole frequency roll-off, and provides output amplifier (output impedance) with output current limit, high current gain (low output impedance), and output short circuit current limit. Bias circuit Provides appropriate quiescent current for each stage of the op amp. (Diode connection) The resistor for connecting Q1 and Q12 (39 k ohms) and the given supply voltage (VS+VS-) determine the current of the current mirror in (match pairs) Q1/Q11 and Q12/Q13. The collector current I_{Q11} , I_{11} is 39 k ohms VS+ / VS- - 2 VBE. For a typical VS+ = 20 V, the standing current I_{Q11} is 1.2 mA. Typ. Input bias current about 2 pA. Differential Amplifier The input phase consists of a cascaded differential amplifier (shown in blue) and an active load on the current mirror. It consists of a transconductance amplifier, which converts the differential voltage signal into a current signal and converts it to a Q15 base at the base of Q1 and Q2. Two cascading transistor pairs are required to meet conflicting requirements. The first phase consists of a matched NPN emitter follower pair Q1, Q2 that provides high input impedance. The second is the matched PNP common base pairs Q3 and Q4, which eliminate undesirable mirror effects. Drives the active load Q7 and matching pairs Q5 and Q6. Its active load will be implemented as the modified Wilson's current mirror. Its role is to convert the (differential) input current signal into a single-ended signal without having to lose 50% of the attendant (increase the open loop gain of the op amp by 3 dB). [nb 4] Therefore, micro signal differential currents of the third and fourth quarters appear(2x) At the base of the Q15, input of the voltage gain stage. The Voltage Amplifier (Class A) Voltage Gain Stage (outlined in Magenta) consists of two NPN transistors Q15/Q19 connected in a Darlington configuration, which uses the output side of the current mirror Q12/Q13 as a collector (dynamic load) to achieve high voltage gain. The output sink transistor Q20 receives the base drive from the common collectors of Q15 and Q19. The LevelShifter Q16 provides the base drive of the output source transistor Q14. Transistor Q22 prevents this stage from supplying excessive current to the Q20 and limits the output sink current. The output amplifier output stage (outlined in Q14, Q20, cyan) is a Class AB complementary symmetry amplifier. It provides an output drive with a current gain, essentially, an impedance of 10 to 50 ohms. Transistor Q16 (shown in green) provides the quiescent current of the output transistor, and Q17 provides the output current limit. Bias circuit Provides appropriate quiescent current for each stage of the op amp. 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(Diode connection) The resistor for connecting Q11 and Q12 (39 k ohms) and the given supply voltage (VS+VS-) determine the current of the current mirror in (match pairs) Q1/Q11 and Q12/Q13. The collector current I_{Q11} , I_{11} is 39 k ohms VS+ / VS- - 2 VBE. For a typical VS+ = 20 V, the standing current I_{Q11} is 1.2 mA. Typ. Input bias current about 2 pA. Differential Amplifier The input phase consists of a cascaded differential amplifier (shown in blue) and an active load on the current mirror. It consists of a transconductance amplifier, which converts the differential voltage signal into a current signal and converts it to a Q15 base at the base of Q1 and Q2. Two cascading transistor pairs are required to meet conflicting requirements. The first phase consists of a matched NPN emitter follower pair Q1, Q2 that provides high input impedance. The second is the matched PNP common base pairs Q3 and Q4, which eliminate undesirable mirror effects. Drives the active load Q7 and matching pairs Q5 and Q6. Its active load will be implemented as the modified Wilson's current mirror. Its role is to convert the (differential) input current signal into a single-ended signal without having to lose 50% of the attendant (increase the open loop gain of the op amp by 3 dB). [nb 4] Therefore, micro signal differential currents of the third and fourth quarters appear(2x) At the base of the Q15, input of the voltage gain stage. The Voltage Amplifier (Class A) Voltage Gain Stage (outlined in Magenta) consists of two NPN transistors Q15/Q19 connected in a Darlington configuration, which uses the output side of the current mirror Q12/Q13 as a collector (dynamic load) to achieve high voltage gain. The output sink transistor Q20 receives the base drive from the common collectors of Q15 and Q19. The LevelShifter Q16 provides the base drive of the output source transistor Q14. Transistor Q22 prevents this stage from supplying excessive current to the Q20 and limits the output sink current. The output amplifier output stage (outlined in Q14, Q20, cyan) is a Class AB complementary symmetry amplifier. It provides an output drive with a current gain, essentially, an impedance of 10 to 50 ohms. Transistor Q16 (shown in green) provides the quiescent current of the output transistor, and Q17 provides the output current limit. Bias circuit Provides appropriate quiescent current for each stage of the op amp. (Diode connection) The resistor for connecting Q11 and Q12 (39 k ohms) and the given supply voltage (VS+VS-) determine the current of the current mirror in (match pairs) Q1/Q11 and Q12/Q13. The collector current I_{Q11} , I_{11} is 39 k ohms VS+ / VS- - 2 VBE. For a typical VS+ = 20 V, the standing current I_{Q11} is 1.2 mA. Typ. Input bias current about 2 pA. Differential Amplifier The input phase consists of a cascaded differential amplifier (shown in blue) and an active load on the current mirror. It consists of a transconductance amplifier, which converts the differential voltage signal into a current signal and converts it to a Q15 base at the base of Q1 and Q2. Two cascading transistor pairs are required to meet conflicting requirements. The first phase consists of a matched NPN emitter follower pair Q1, Q2 that provides high input impedance. The second is the matched PNP common base pairs Q3 and Q4, which eliminate undesirable mirror effects. Drives the active load Q7 and matching pairs Q5 and Q6. Its active load will be implemented as the modified Wilson's current mirror. Its role is to convert the (differential) input current signal into a single-ended signal without having to lose 50% of the attendant (increase the open loop gain of the op amp by 3 dB). [nb 4] Therefore, micro signal differential currents of the third and fourth quarters appear(2x) At the base of the Q15, input of the voltage gain stage. The Voltage Amplifier (Class A) Voltage Gain Stage (outlined in Magenta) consists of two NPN transistors Q15/Q19 connected in a Darlington configuration, which uses the output side of the current mirror Q12/Q13 as a collector (dynamic load) to achieve high voltage gain. The output sink transistor Q20 receives the base drive from the common collectors of Q15 and Q19. The LevelShifter Q16 provides the base drive of the output source transistor Q14. Transistor Q22 prevents this stage from supplying excessive current to the Q20 and limits the output sink current. The output amplifier output stage (outlined in Q14, Q20, cyan) is a Class AB complementary symmetry amplifier. It provides an output drive with a current gain, essentially, an impedance of 10 to 50 ohms. Transistor Q16 (shown in green) provides the quiescent current of the output transistor, and Q17 provides the output current limit. Bias circuit Provides appropriate quiescent current for each stage of the op amp. (Diode connection) The resistor for connecting Q11 and Q12 (39 k ohms) and the given supply voltage (VS+VS-) determine the current of the current mirror in (match pairs) Q1/Q11 and Q12/Q13. The collector current I_{Q11} , I_{11} is 39 k ohms VS+ / VS- - 2 VBE. For a typical VS+ = 20 V, the standing current I_{Q11} is 1.2 mA. Typ. Input bias current about 2 pA. Differential Amplifier The input phase consists of a cascaded differential amplifier (shown in blue) and an active load on the current mirror. It consists of a transconductance amplifier, which converts the differential voltage signal into a current signal and converts it to a Q15 base at the base of Q1 and Q2. Two cascading transistor pairs are required to meet conflicting requirements. The first phase consists of a matched NPN emitter follower pair Q1, Q2 that provides high input impedance. The second is the matched PNP common base pairs Q3 and Q4, which eliminate undesirable mirror effects. Drives the active load Q7 and matching pairs Q5 and Q6. Its active load will be implemented as the modified Wilson's current mirror. Its role is to convert the (differential) input current signal into a single-ended signal without having to lose 50% of the attendant (increase the open loop gain of the op amp by 3 dB). [nb 4] Therefore, micro signal differential currents of the third and fourth quarters appear(2x) At the base of the Q15, input of the voltage gain stage. The Voltage Amplifier (Class A) Voltage Gain Stage (outlined in Magenta) consists of two NPN transistors Q15/Q19 connected in a Darlington configuration, which uses the output side of the current mirror Q12/Q13 as a collector (dynamic load) to achieve high voltage gain. The output sink transistor Q20 receives the base drive from the common collectors of Q15 and Q19. The LevelShifter Q16 provides the base drive of the output source transistor Q14. Transistor Q22 prevents this stage from supplying excessive current to the Q20 and limits the output sink current. The output amplifier output stage (outlined in Q14, Q20, cyan) is a Class AB complementary symmetry amplifier. It provides an output drive with a current gain, essentially, an impedance of 10 to 50 ohms. Transistor Q16 (shown in green) provides the quiescent current of the output transistor, and Q17 provides the output current limit. Bias circuit Provides appropriate quiescent current for each stage of the op amp. (Diode connection) The resistor for connecting Q11 and Q12 (39 k ohms) and the given supply voltage (VS+VS-) determine the current of the current mirror in (match pairs) Q1/Q11 and Q12/Q13. The collector current I_{Q11} , I_{11} is 39 k ohms VS+ / VS- - 2 VBE. For a typical VS+ = 20 V, the standing current I_{Q11} is 1.2 mA. Typ. Input bias current about 2 pA. Differential Amplifier The input phase consists of a cascaded differential amplifier (shown in blue) and an active load on the current mirror. It consists of a transconductance amplifier, which converts the differential voltage signal into a current signal and converts it to a Q15 base at the base of Q1 and Q2. Two cascading transistor pairs are required to meet conflicting requirements. The first phase consists of a matched NPN emitter follower pair Q1, Q2 that provides high input impedance. The second is the matched PNP common base pairs Q3 and Q4, which eliminate undesirable mirror effects. Drives the active load Q7 and matching pairs Q5 and Q6. Its active load will be implemented as the modified Wilson's current mirror. Its role is to convert the (differential) input current signal into a single-ended signal without having to lose 50% of the attendant (increase the open loop gain of the op amp by 3 dB). [nb 4] Therefore, micro signal differential currents of the third and fourth quarters appear(2x) At the base of the Q15, input of the voltage gain stage. The Voltage Amplifier (Class A) Voltage Gain Stage (outlined in Magenta) consists of two NPN transistors Q15/Q19 connected in a Darlington configuration, which uses the output side of the current mirror Q12/Q13 as a collector (dynamic load) to achieve high voltage gain. The output sink transistor Q20 receives the base drive from the common collectors of Q15 and Q19. The LevelShifter Q16 provides the base drive of the output source transistor Q14. Transistor Q22 prevents this stage from supplying excessive current to the Q20 and limits the output sink current. The output amplifier output stage (outlined in Q14, Q20, cyan) is a Class AB complementary symmetry amplifier. It provides an output drive with a current gain, essentially, an impedance of 10 to 50 ohms. Transistor Q16 (shown in green) provides the quiescent current of the output transistor, and Q17 provides the output current limit. Bias circuit Provides appropriate quiescent current for each stage of the op amp. (Diode connection) The resistor for connecting Q11 and Q12 (39 k ohms) and the given supply voltage (VS+VS-) determine the current of the current mirror in (match pairs) Q1/Q11 and Q12/Q13. The collector current I_{Q11} , I_{11} is 39 k ohms VS+ / VS- - 2 VBE. For a typical VS+ = 20 V, the standing current I_{Q11} is 1.2 mA. Typ. Input bias current about 2 pA. Differential Amplifier The input phase consists of a cascaded differential amplifier (shown in blue) and an active load on the current mirror. It consists of a transconductance amplifier, which converts the differential voltage signal into a current signal and converts it to a Q15 base at the base of Q1 and Q2. Two cascading transistor pairs are required to meet conflicting requirements. The first phase consists of a matched NPN emitter follower pair Q1, Q2 that provides high input impedance. The second is the matched PNP common base pairs Q3 and Q4, which eliminate undesirable mirror effects. Drives the active load Q7 and matching pairs Q5 and Q6. Its active load will be implemented as the modified Wilson's current mirror. Its role is to convert the (differential) input current signal into a single-ended signal without having to lose 50% of the attendant (increase the open loop gain of the op amp by 3 dB). [nb 4] Therefore, micro signal differential currents of the third and fourth quarters appear(2x) At the base of the Q15, input of the voltage gain stage. The Voltage Amplifier (Class A) Voltage Gain Stage (outlined in Magenta) consists of two NPN transistors Q15/Q19 connected in a Darlington configuration, which uses the output side of the current mirror Q12/Q13 as a collector (dynamic load) to achieve high voltage gain. The output sink transistor Q20 receives the base drive from the common collectors of Q15 and Q19. The LevelShifter Q16 provides the base drive of the output source transistor Q14. Transistor Q22 prevents this stage from supplying excessive current to the Q20 and limits the output sink current. The output amplifier output stage (outlined in Q14, Q20, cyan) is a Class AB complementary symmetry amplifier. It provides an output drive with a current gain, essentially, an impedance of 10 to 50 ohms. Transistor Q16 (shown in green) provides the quiescent current of the output transistor, and Q17 provides the output current limit. Bias circuit Provides appropriate quiescent current for each stage of the op amp. (Diode connection) The resistor for connecting Q11 and Q12 (39 k ohms) and the given supply voltage (VS+VS-) determine the current of the current mirror in (match pairs) Q1/Q11 and Q12/Q13. The collector current I_{Q11} , I_{11} is 39 k ohms VS+ / VS- - 2 VBE. For a typical VS+ = 20 V, the standing current I_{Q11} is 1.2 mA. Typ. Input bias current about 2 pA. Differential Amplifier The input phase consists of a cascaded differential amplifier (shown in blue) and an active load on the current mirror. It consists of a transconductance amplifier, which converts the differential voltage signal into a current signal and converts it to a Q15 base at the base of Q1 and Q2. Two cascading transistor pairs are required to meet conflicting requirements. The first phase consists of a matched NPN emitter follower pair Q1, Q2 that provides high input impedance. The second is the matched PNP common base pairs Q3 and Q4, which eliminate undesirable mirror effects. Drives the active load Q7 and matching pairs Q5 and Q6. Its active load will be implemented as the modified Wilson's current mirror. Its role is to convert the (differential) input current signal into a single-ended signal without having to lose 50% of the attendant (increase the open loop gain of the op amp by 3 dB). [nb 4] Therefore, micro signal differential currents of the third and fourth quarters appear(2x) At the base of the Q15, input of the voltage gain stage. The Voltage Amplifier (Class A) Voltage Gain Stage (outlined in Magenta) consists of two NPN transistors Q15/Q19 connected in a Darlington configuration, which uses the output side of the current mirror Q12/Q13 as a collector (dynamic load) to achieve high voltage gain. The output sink transistor Q20 receives the base drive from the common collectors of Q15 and Q19. The LevelShifter Q16 provides the base drive of the output source transistor Q14. Transistor Q22 prevents this stage from supplying excessive current to the Q20 and limits the output sink current. The output amplifier output stage (outlined in Q14, Q20, cyan) is a Class AB complementary symmetry amplifier. It provides an output drive with a current gain, essentially, an impedance of 10 to 50 ohms. Transistor Q16 (shown in green) provides the quiescent current of the output transistor, and Q17 provides the output current limit. Bias circuit Provides appropriate quiescent current for each stage of the op amp. (Diode connection) The resistor for connecting Q11 and Q12 (39 k ohms) and the given supply voltage (VS+VS-) determine the current of the current mirror in (match pairs) Q1/Q11 and Q12/Q13. The collector current I_{Q11} , I_{11} is 39 k ohms VS+ / VS- - 2 VBE. For a typical VS+ = 20 V, the standing current I_{Q11} is 1.2 mA. Typ. Input bias current about 2 pA. Differential Amplifier The input phase consists of a cascaded differential amplifier (shown in blue) and an active load on the current mirror. It consists of a transconductance amplifier, which converts the differential voltage signal into a current signal and converts it to a Q15 base at the base of Q1 and Q2. Two cascading transistor pairs are required to meet conflicting requirements. The first phase consists of a matched NPN emitter follower pair Q1, Q2 that provides high input impedance. The second is the matched PNP common base pairs Q3 and Q4, which eliminate undesirable mirror effects. Drives the active load Q7 and matching pairs Q5 and Q6. Its active load will be implemented as the modified Wilson's current mirror. Its role is to convert the (differential) input current signal into a single-ended signal without having to lose 50% of the attendant (increase the open loop gain of the op amp by 3 dB). [nb 4] Therefore, micro signal differential currents of the third and fourth quarters appear(2x) At the base of the Q15, input of the voltage gain stage. The Voltage Amplifier (Class A) Voltage Gain Stage (outlined in Magenta) consists of two NPN transistors Q15/Q19 connected in a Darlington configuration, which uses the output side of the current mirror Q12/Q13 as a collector (dynamic load) to achieve high voltage gain. The output sink transistor Q20 receives the base drive from the common collectors of Q15 and Q19. The LevelShifter Q16 provides the base drive of the output source transistor Q14. Transistor Q22 prevents this stage from supplying excessive current to the Q20 and limits the output sink current. The output amplifier output stage (outlined in Q14, Q20, cyan) is a Class AB complementary symmetry amplifier. It provides an output drive with a current gain, essentially, an impedance of 10 to 50 ohms. Transistor Q16 (shown in green) provides the quiescent current of the output transistor, and Q17 provides the output current limit. Bias circuit Provides appropriate quiescent current for each stage of the op amp. (Diode connection) The resistor for connecting Q11 and Q12 (39 k ohms) and the given supply voltage (VS+VS-) determine the current of the current mirror in (match

